

Synchronizing Behavioural Mismatch in Software Composition

Carlos Canal



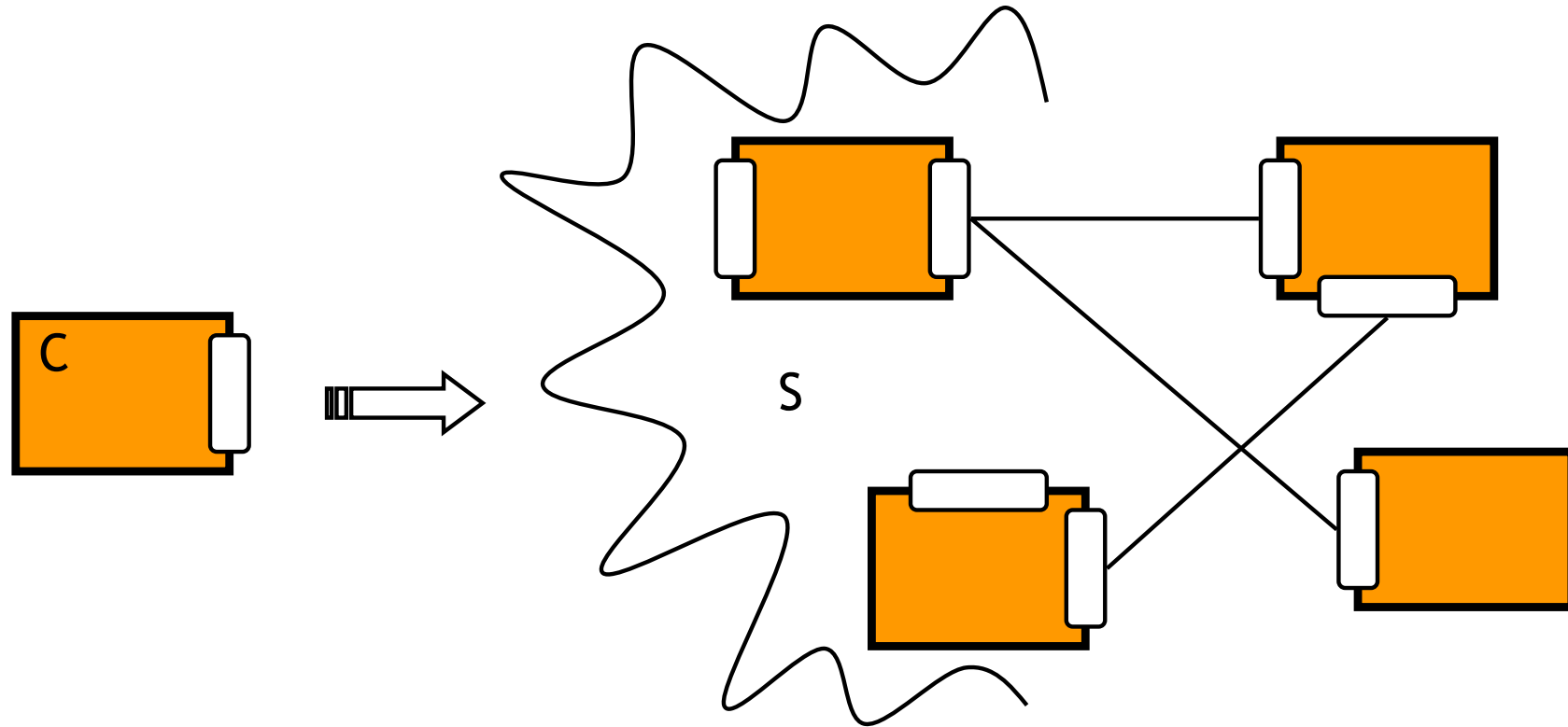
Pascal Poizat



Gwen Salaün

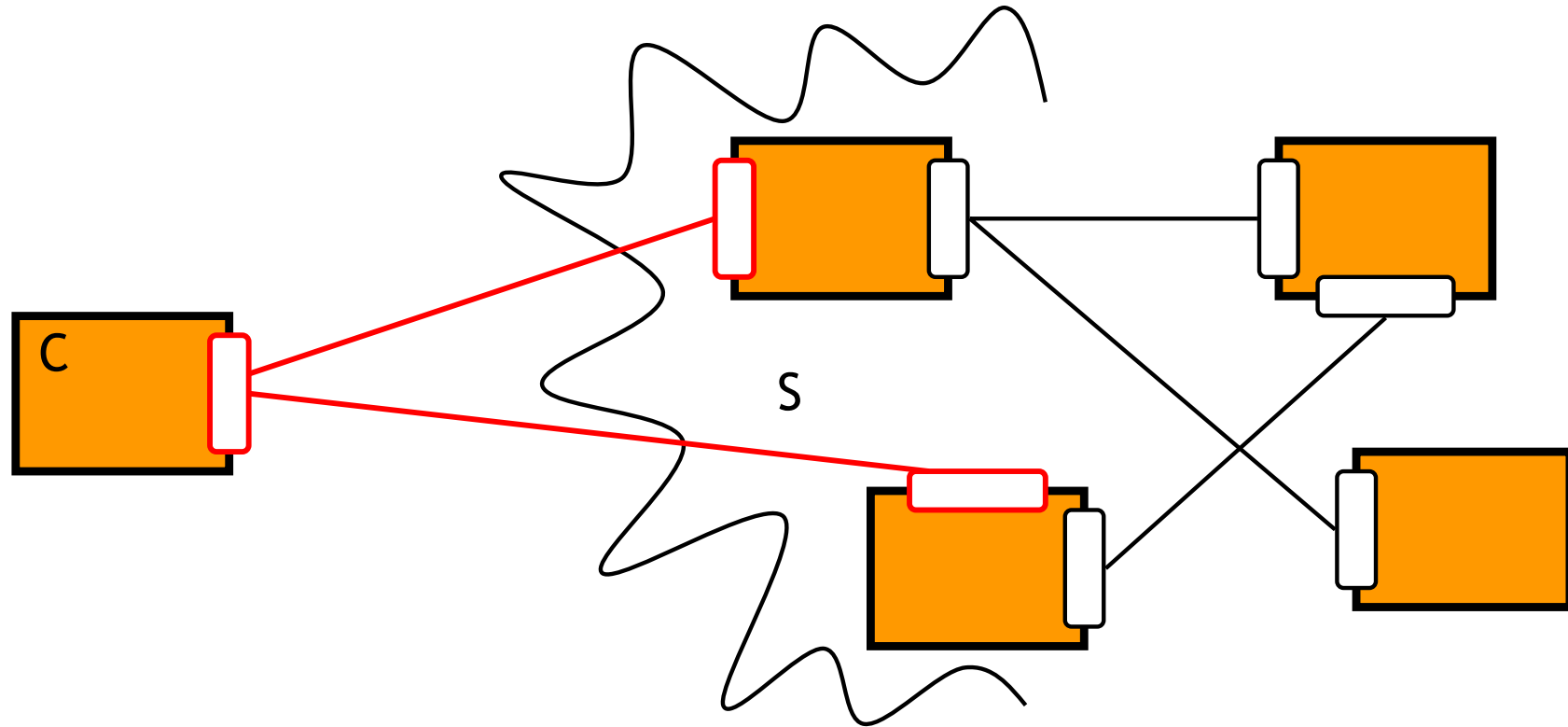


Composition Scenario



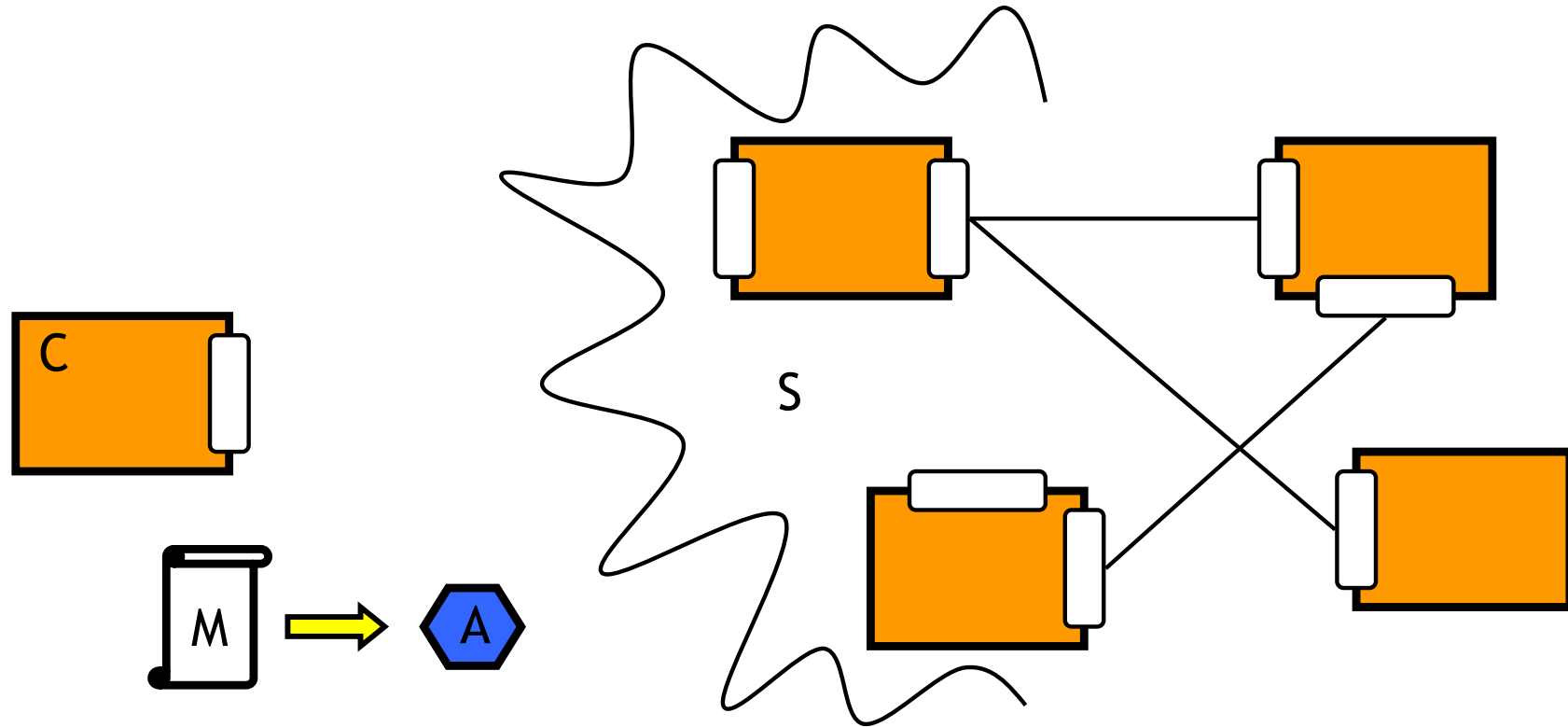
- Addition of a component C to the system S

Composition Scenario



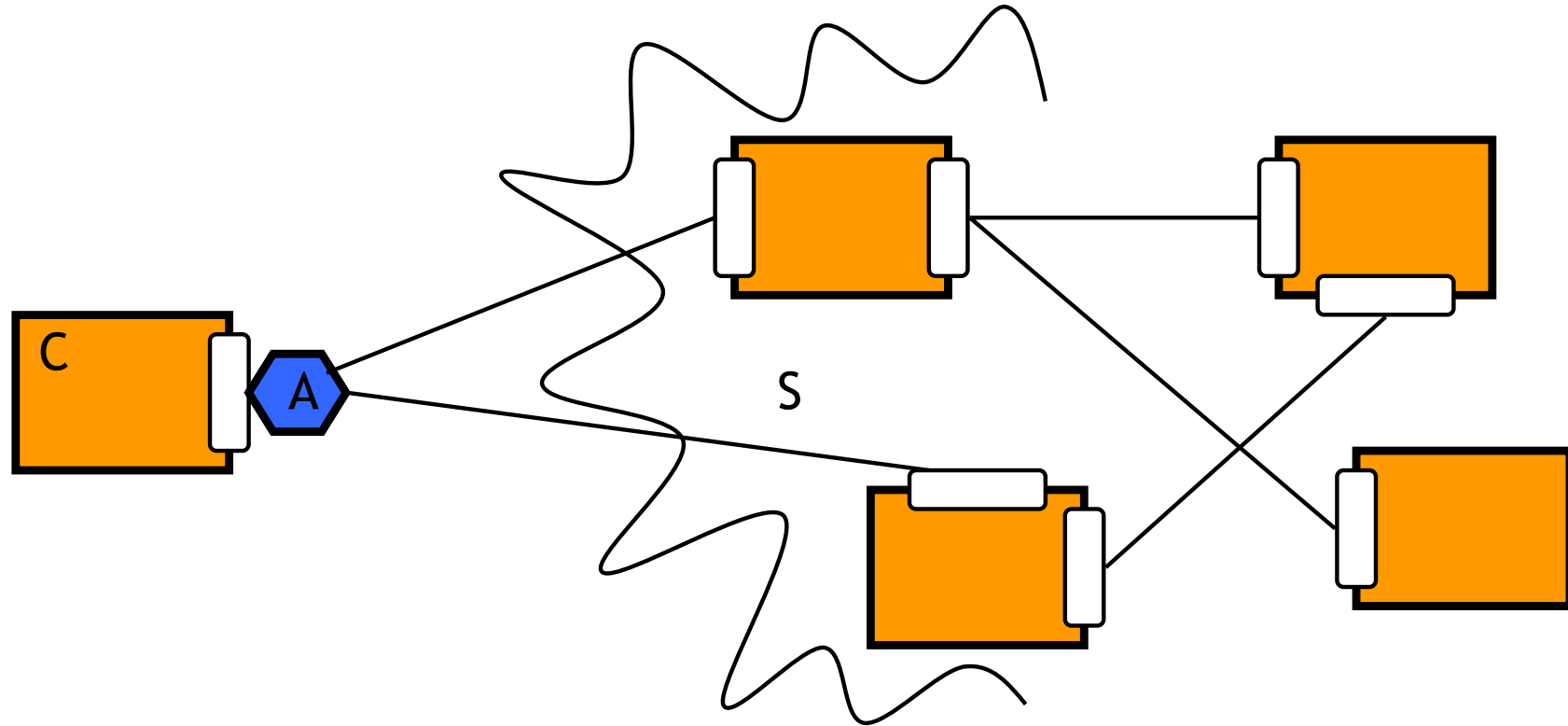
- Addition of a component C to the system S
- Connection is not possible: $C|S$ is blocking!

Composition Scenario



- Addition of a component **C** to the system **S**
- Connection is not possible: $C|S$ is blocking!
- Generation of an adaptor **A** using a mapping **M**

Composition Scenario



- Addition of a component C to the system S
- Connection is not possible: $C|S$ is blocking!
- Generation of an adaptor A using a mapping
- The system $C|A|S$ is not blocking

Motivation

- Component-based systems are built by composition and reuse of existing components
- Several levels of **interoperability** which may raise incompatibilities:
 - + Signatures, **behaviours**
 - Semantic aspects, quality of services
- A component is seldom used directly as it is and needs some **adaptations**
- Reusing components **as automatically as possible**

Outline of the Presentation

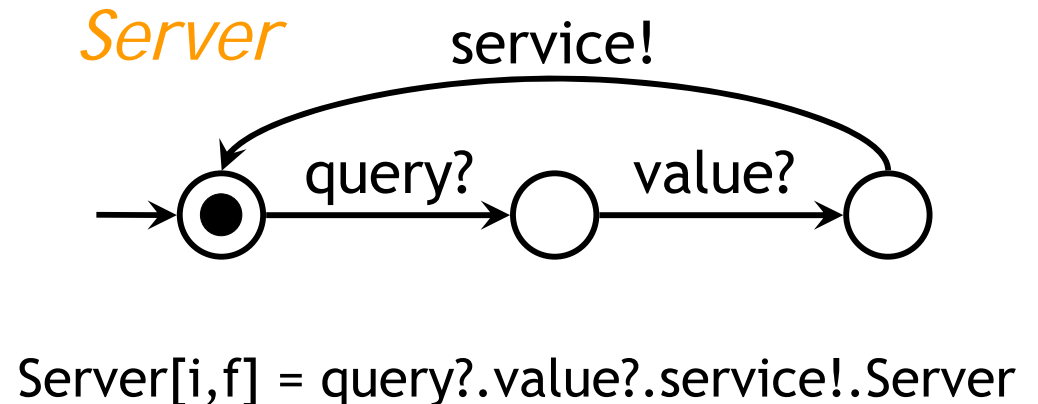
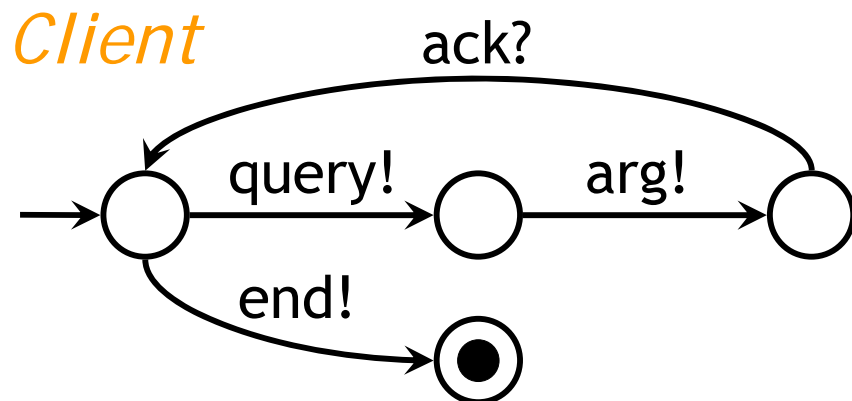
- Overview of our Approach
- Adaptation using Vectors
- Adaptation using Regular Expressions
- Conclusion and Future Work
- Demo

Behavioural Interfaces (BIDL)

- Signatures of operations
- **LTS** : (A, S, I, F, T)
- Simple **process algebra** (sequential CCS):

$$P ::= 0 \mid m!.P \mid m?.P \mid P1+P2 \mid A$$

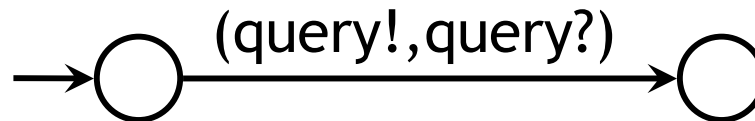
with [i] and [f] for initial and final states



Compatibility Check

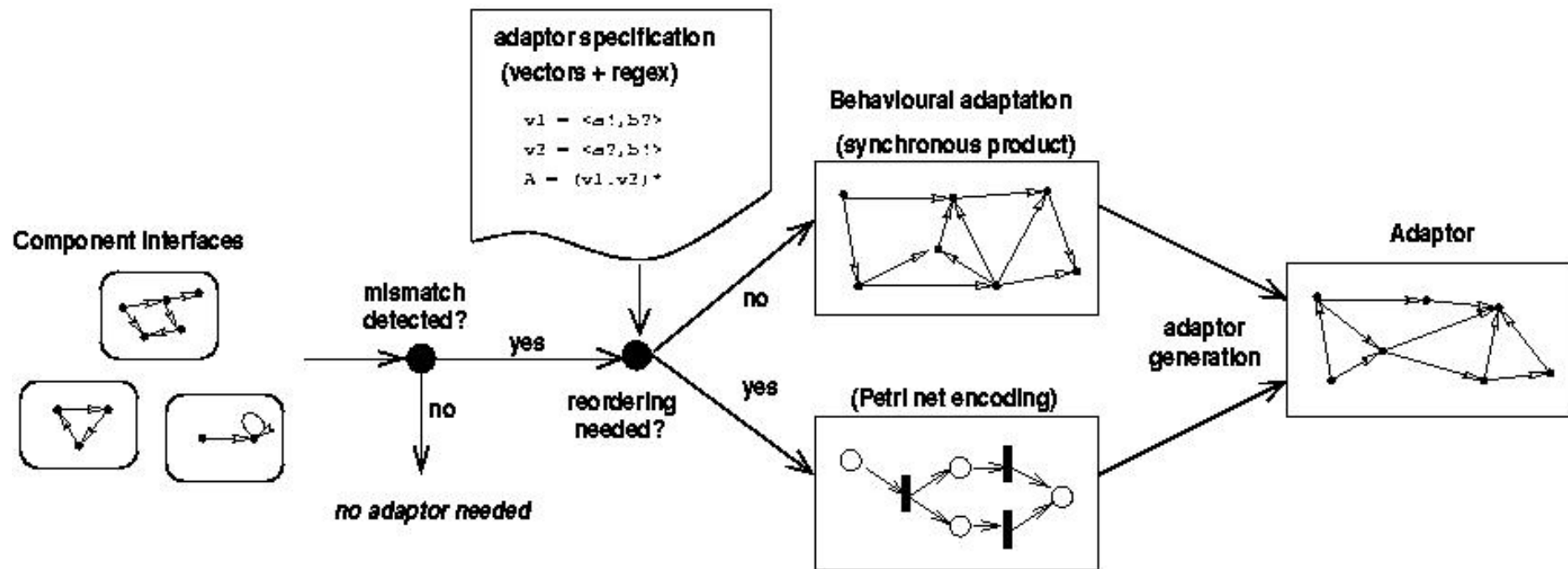
- **Synchronized product** [Arnold94] to build a unique LTS from several LTS components
- A **deadlock** in a LTS if one state is reachable yet not final
- Several components are **compatible** if the product of their interfaces is **deadlock-free**

Client / Server



This state is not final!

Overview of our Approach

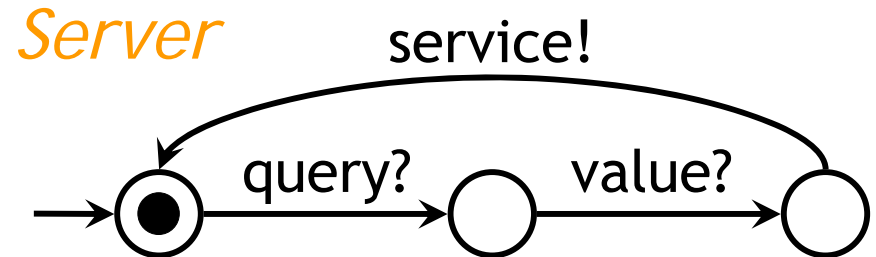
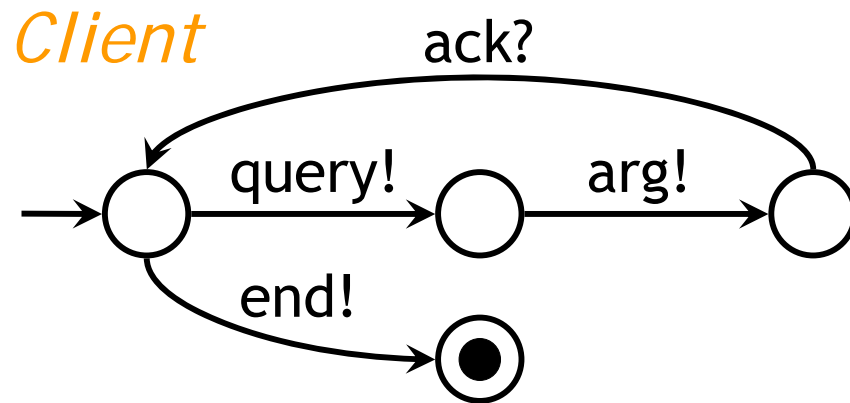


Outline of the Talk

- Overview of our Approach
- **Adaptation using Vectors**
- Adaptation using Regular Expressions
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Synchronization Vectors

- Being given a set of LTS $L_i = (A_i, S_i, I_i, F_i, T_i)$, a **vector** is a tuple $\langle e_i \rangle$ with $e_i \in A_i \cup \{\varepsilon\}$
- Example:



- Vectors:

$\langle c:\text{query!}, s:\text{query?} \rangle$

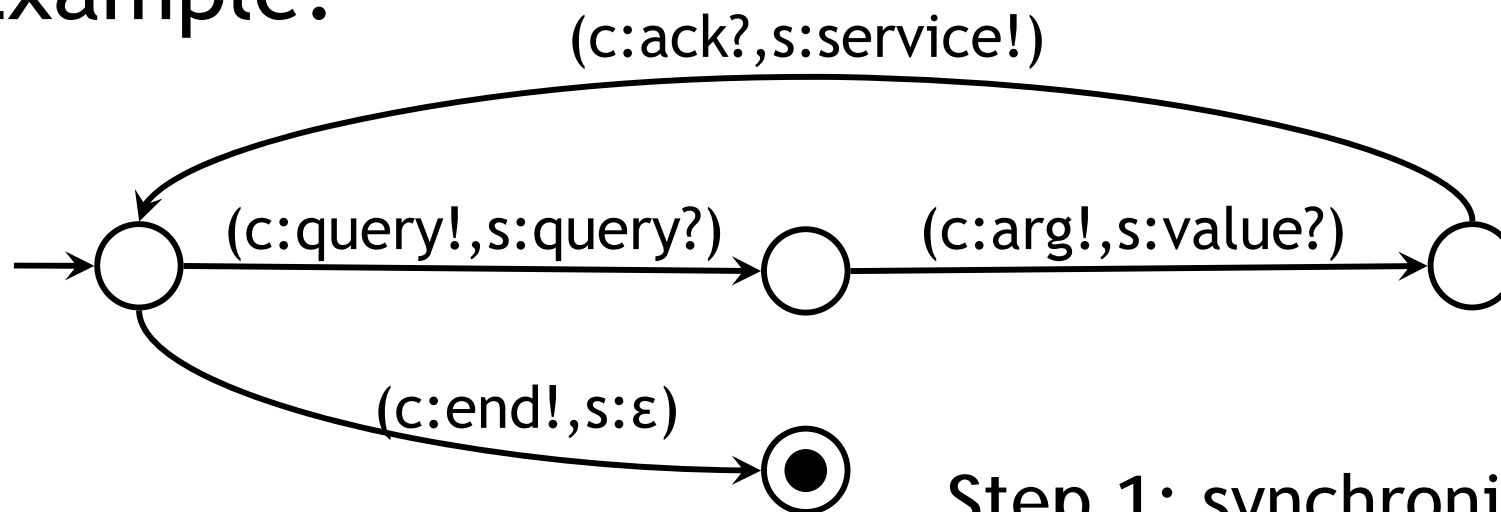
$\langle c:\text{ack?}, s:\text{service!} \rangle$

$\langle c:\text{arg!}, s:\text{value?} \rangle$

$\langle c:\text{end!}, s:\varepsilon \rangle$

Adaptation without Reordering

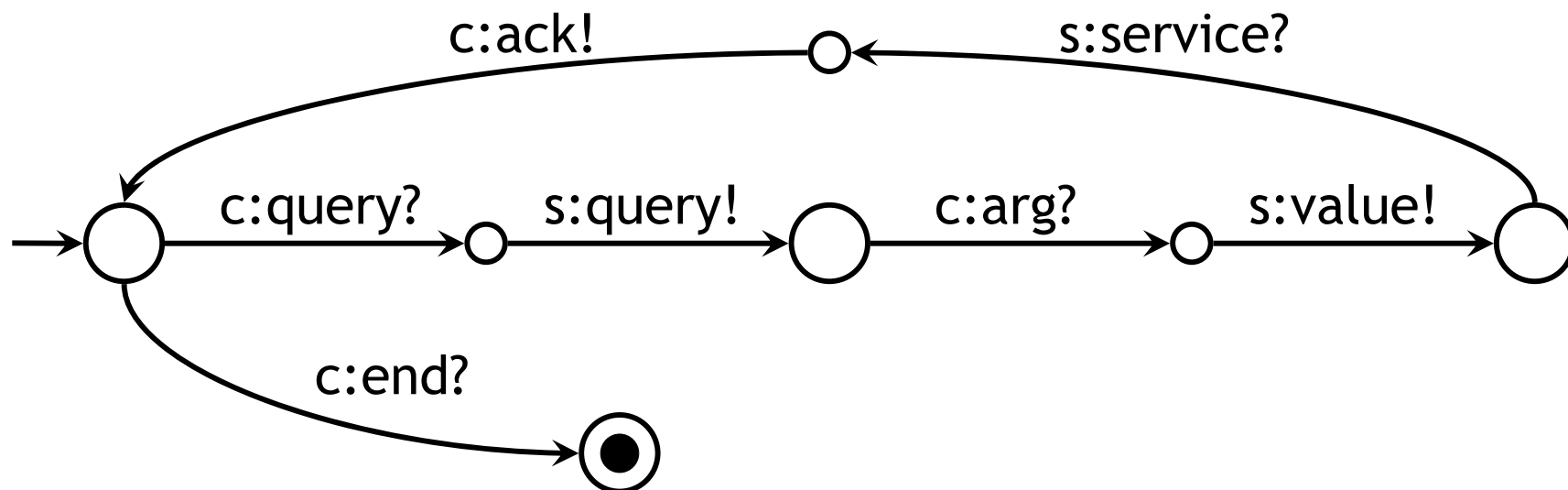
- Algorithm:
 - Compute the **synchronized product** from LTS L_i and vectors V
 - Remove paths to deadlock
 - Compute permutations and reverse actions
- Example:



Step 1: synchronized product

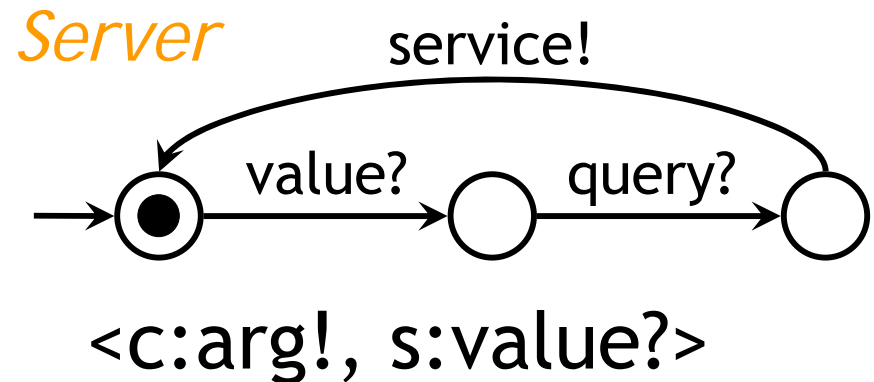
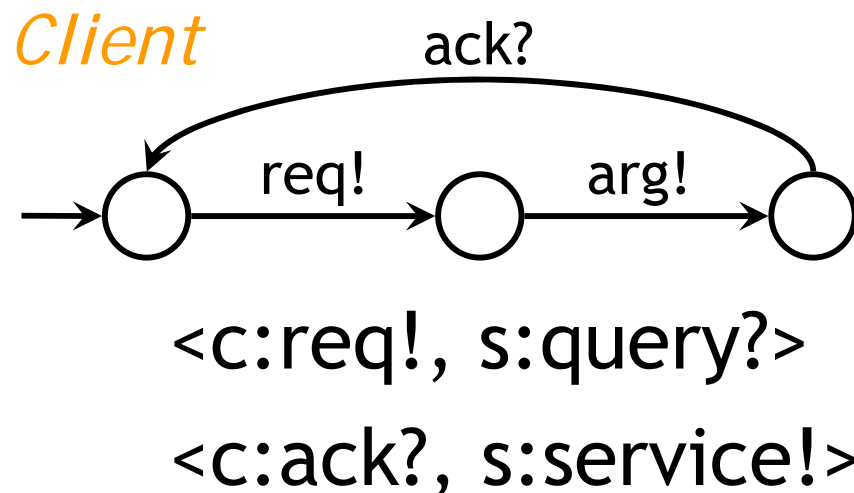
Adaptation without Reordering

- Step 2: no deadlock to remove
- Step 3: reverse actions



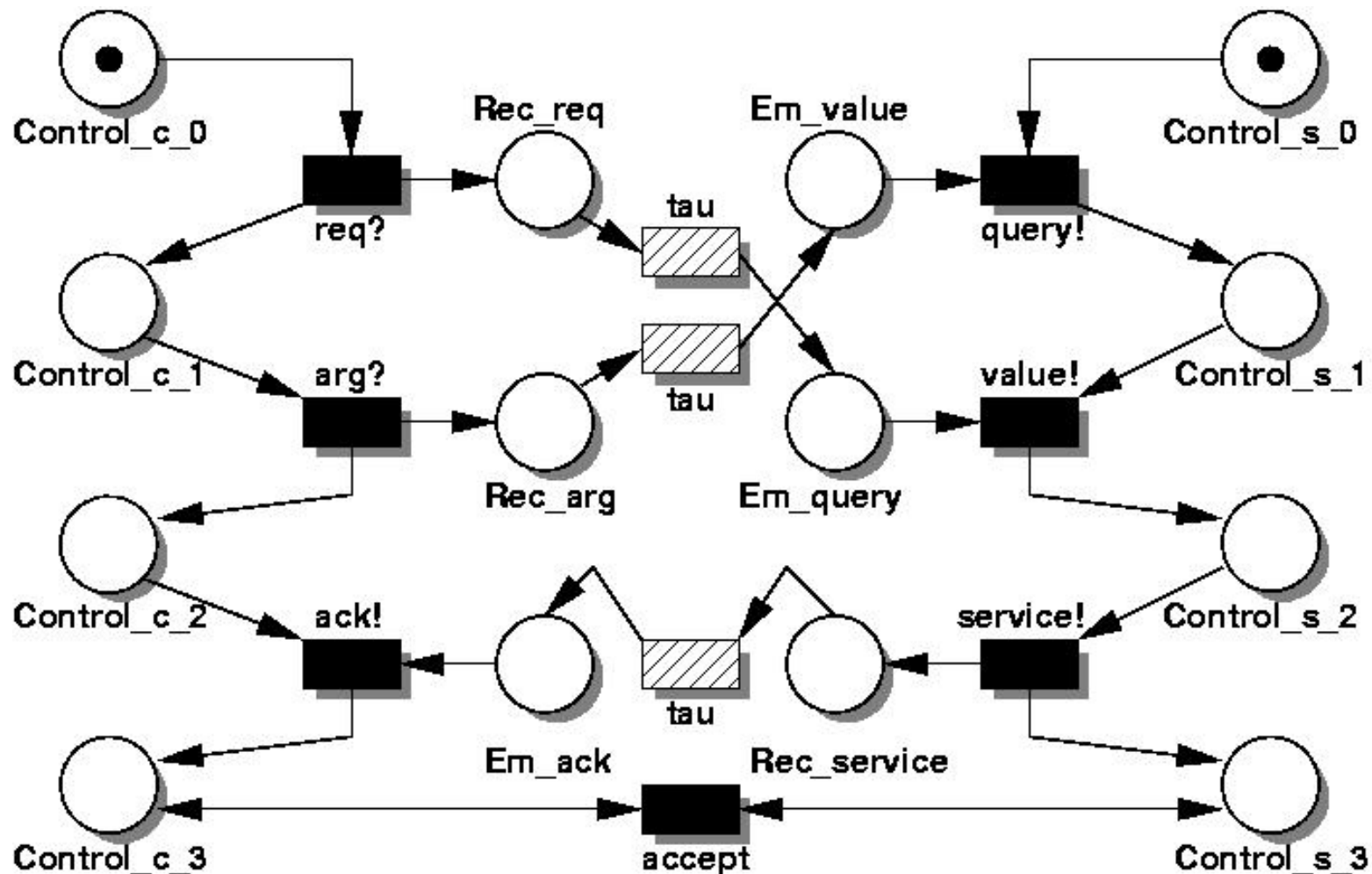
Adaptation with Reordering

- Algorithm:
 - Encode all LTSs and vectors V into Petri nets
 - Compute marking / cover graph (TINA)
 - Remove paths to deadlock
 - Apply reduction on adaptor to remove τ (CADP)
- Example:



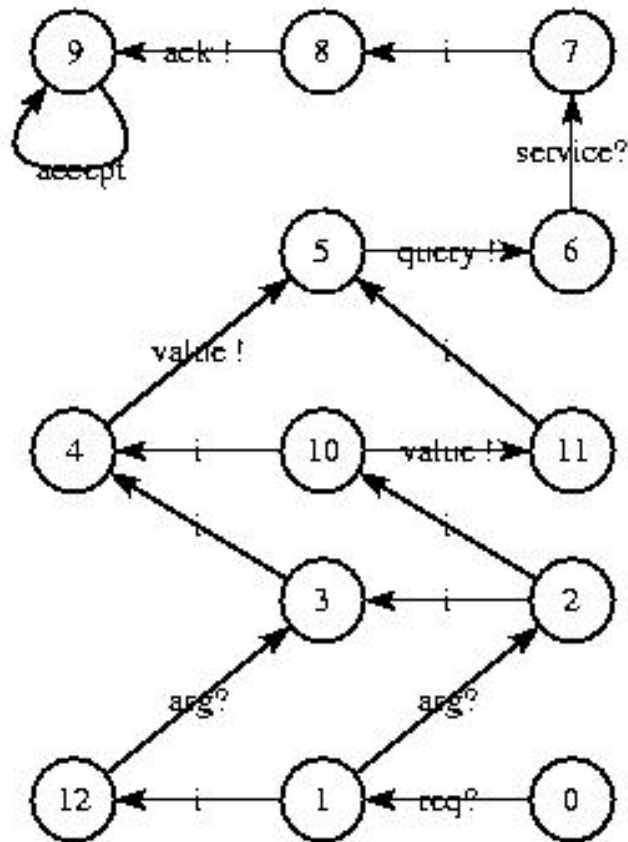
Adaptation with Reordering

- Step 1: encoding into Petri nets

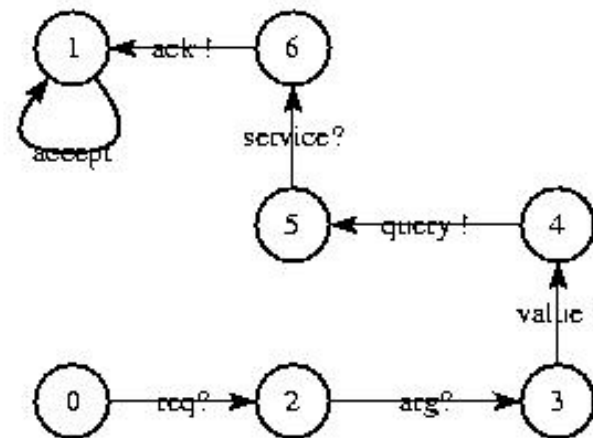


Adaptation with Reordering

- Step 2: marking graph computation



- Step 3: no deadlock to remove
- Step 4: reduction to remove τ actions



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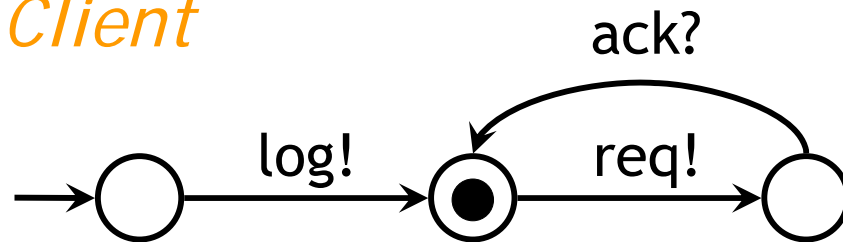
Regular Expressions

- Ordering needed: regular expressions of vectors

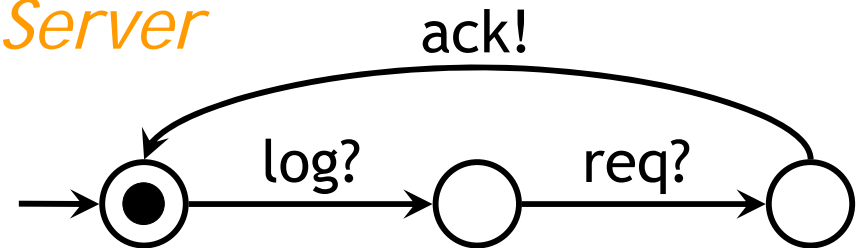
$R ::= v \mid R1.R2 \text{ (SEQ)} \mid R1+R2 \text{ (CH)} \mid R^* \text{ (ITER)}$

- Example:

Client



Server



- Vectors:

$v_0 = \langle c:\text{log!}, s:\text{log?} \rangle$

$v_1 = \langle c:\epsilon, s:\text{log?} \rangle$

$v_2 = \langle c:\text{req!}, s:\text{req?} \rangle$

$v_3 = \langle c:\text{ack?}, s:\text{ack!} \rangle$

- Regexp: $v_0 \cdot v_2 \cdot v_3 \cdot (v_1 \cdot v_2 \cdot v_3)^*$

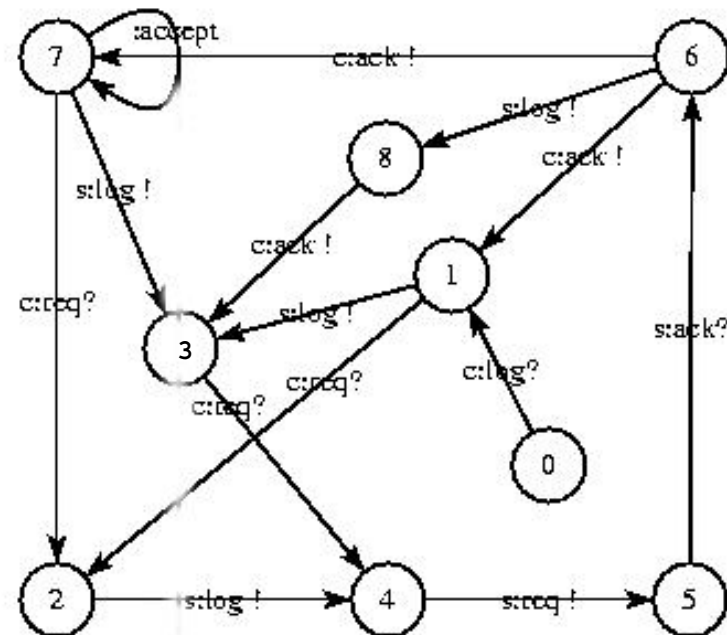


Adaptation without Reordering

- Algorithm: replace Step 1 of Vectors algo by
 - Compute the LTS L_R for the regexp R
 - Compute the synchronized product from LTS L_i and LTS L_R
 - Discard elements of R in the resulting LTS

- Example:

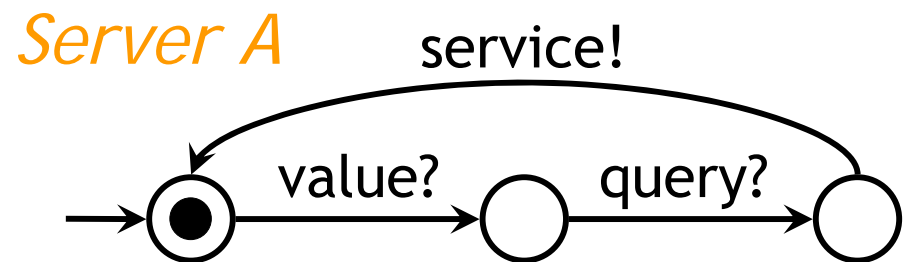
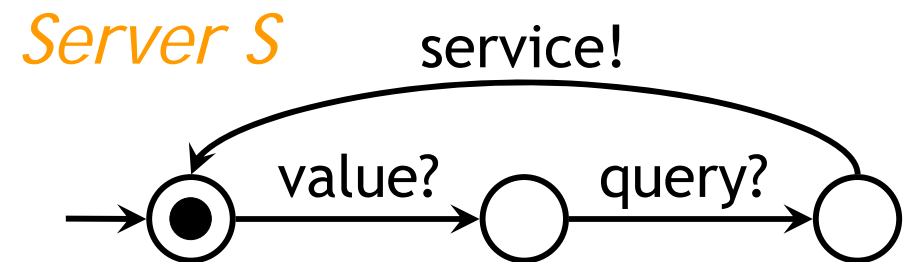
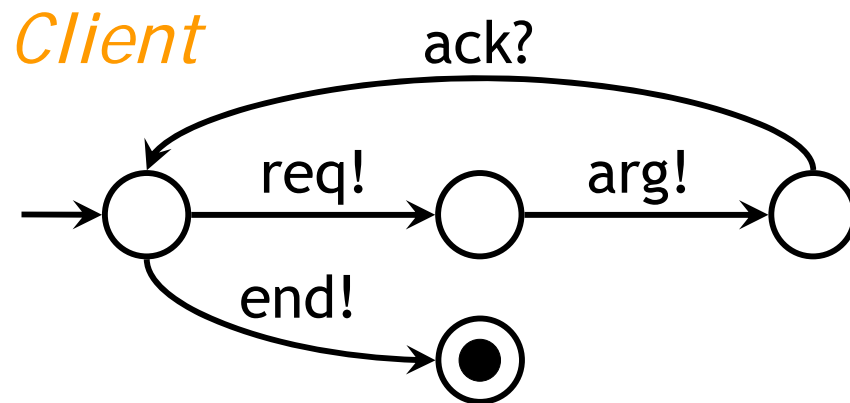
Abstract adaptor 



Adaptation with Reordering

- Algorithm: replace Step 1 of Vectors algo by
 - Encode all LTSs and the LTS L_R of the regexp R into Petri nets

Example:



$$V_{s1} = \langle c: req!, s: query?, a: \epsilon \rangle$$

$$V_{a1} = \langle \dots \rangle$$

$$V_{s2} = \langle c: arg!, s: value?, a: \epsilon \rangle$$

$$V_{a2} = \langle \dots \rangle$$

$$V_{s3} = \langle c: ack?, s: service!, a: \epsilon \rangle$$

$$V_{a3} = \langle \dots \rangle$$

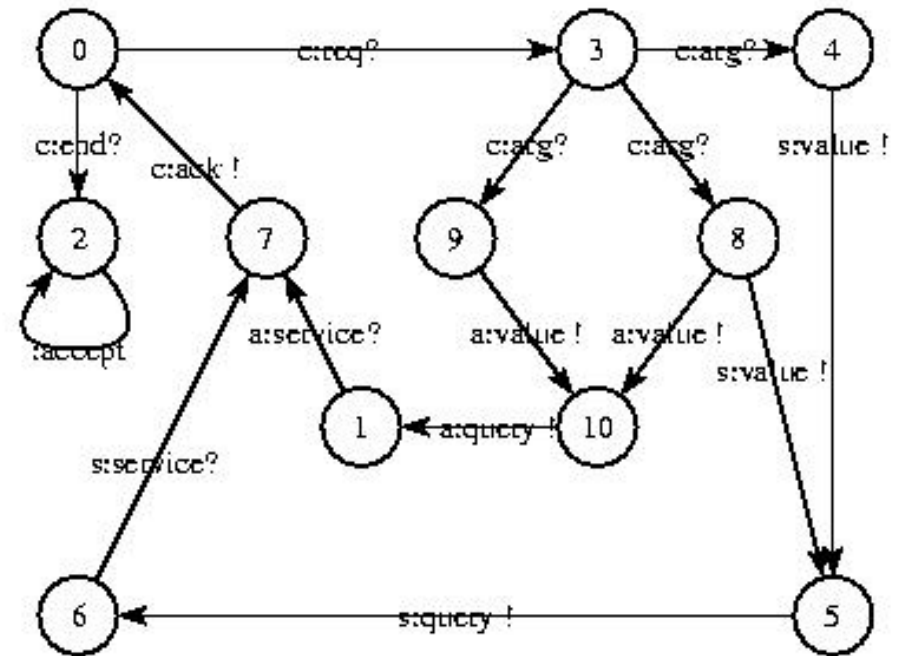
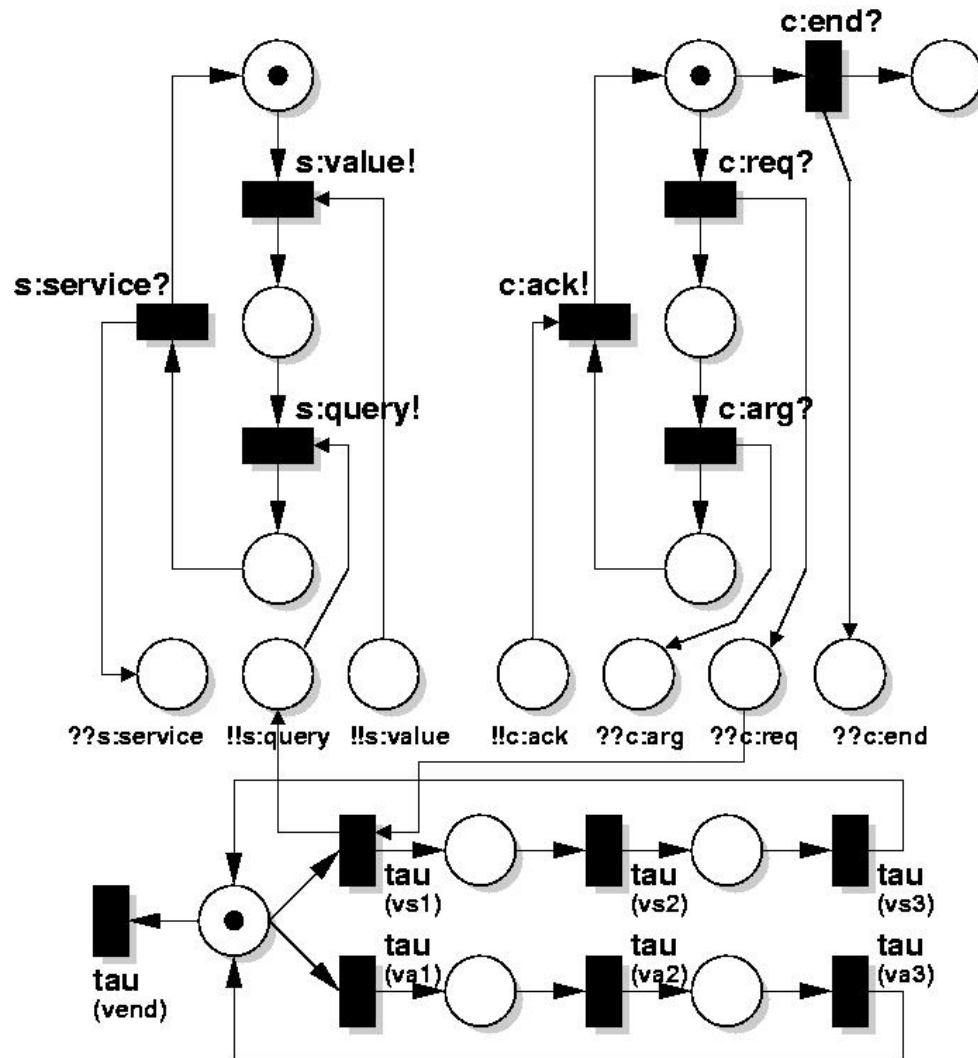
$$V_{end} = \langle c: end!, s: \epsilon, a: \epsilon \rangle$$

Regexp:

$$(V_{s1} \cdot V_{s2} \cdot V_{s3} + V_{a1} \cdot V_{a2} \cdot V_{a3})^* \cdot V_{end}$$

Adaptation with Reordering

- Encoding into Petri nets and abstract adaptor



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Conclusion

- An approach for component adaptation based on **vectors** and **regular expressions**
- Supported by algorithms and tools:
 - **CADP**: compatibility check, τ -reductions
 - **TINA**: Petri nets marking and cover graphs
- Fully automated by a prototype (**ADAPTOR**)
 - \Rightarrow a demo is coming soon!
- Significant insight compared to existing related works...

Comparison with Related Work

Criteria	Inverardi & Tivoli	Brogi et al.	Ours
BIDL	Automata	Proc. algebra	LTS Proc. Algebra
Properties	No deadlock LTL	No deadlock	No deadlock Regexp
Abstraction	Yes	Yes	Yes
Incomp. names	No	Yes	Yes
Data	No	Yes	No
Reordering	No	Yes	Yes
System	Yes	No	Yes
Tools	Yes	No	Yes



Future Work

- Adaptations of messages with data
- Extending our approach with semantic aspects or quality of services (resources, time)
- Automating the generation of mappings
- Formal proof of the algorithms correction
- Connection with implementation component models

Demo

(by Pascal Poizat)

