

### Quantitative Evaluation in Embedded System Design

## Validation of Multiprocessor Multithreaded Architecture

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- Introduction
- The MULTIVAL project
  - Validation of distributed and asynchronous systems
  - The CADP toolbox
- Performance evaluation
  - From LOTOS to Markov chains
  - Methodology
  - Example : a simplified xSTream queue
- Conclusion

## Introduction

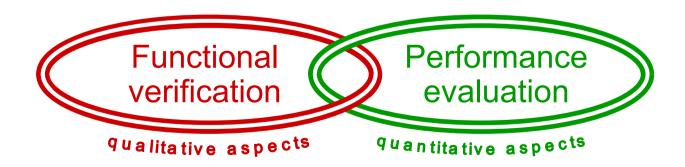
- Asynchronous computing becomes widely used:
  - Increased computing performances
  - Increased flexibility and scalability
  - Energy consumption optimization
- Asynchronous computing is found at many levels:
  - Grids, clusters
  - Multiprocessor architectures
  - Multicore processors
  - Asynchronous logic

# Introduction

Challenges in distributed system design:

- Break with the synchronous design approach
- High functional complexity
  - → functional verification more difficult
  - $\rightarrow$  no industrial methodology

- High degree of concurrency
  - → communication latencies may appear
  - → but time constraints have to be respected

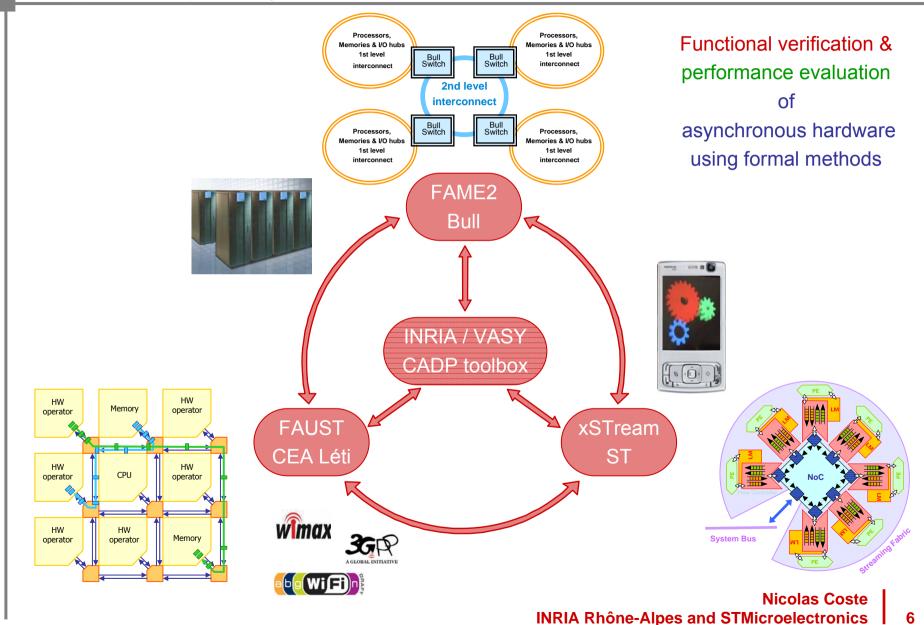




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## **MINALOGIC / MULTIVAL**

http://www.inrialpes.fr/vasy/multival/

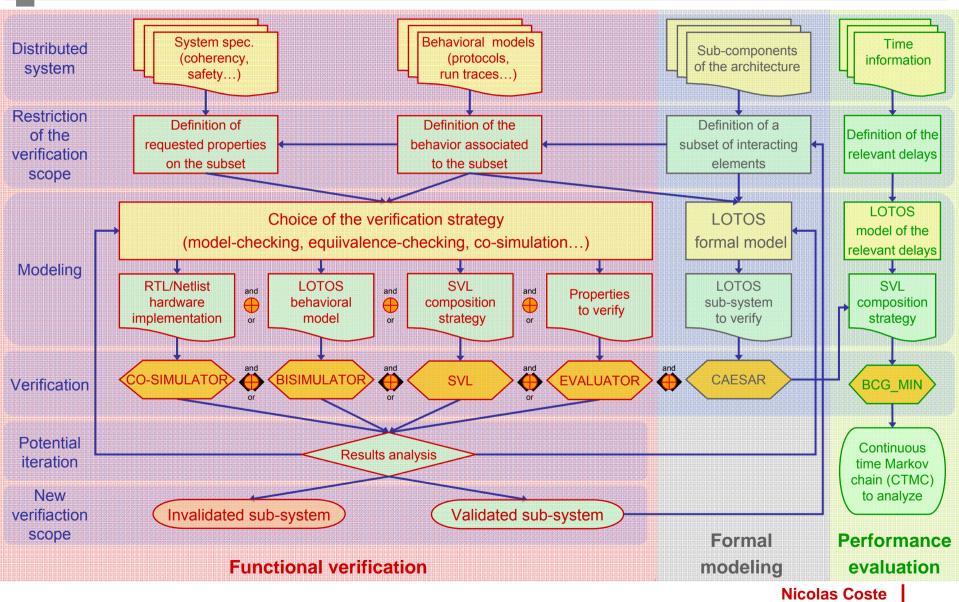




#### • Formal modeling of asynchronous systems

- Formal models of the architecture behaviors
- High-level languages translated into LOTOS (ISO 8807)
- CADP tools helping hardware conception :
  - Compilers, translators and model generators
  - Functional verification :
    - Model checking, equivalence checking
    - Co-simulation (RTL LOTOS)
  - Performance evaluation :
    - Functional models enriched with time information. Performance evaluation based on IMC theory.

# **CADP** methodology

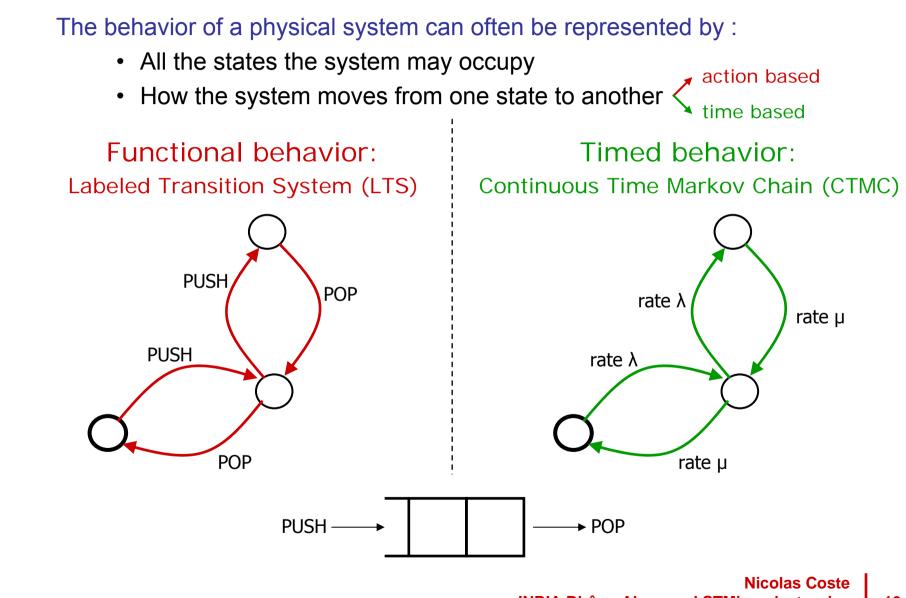


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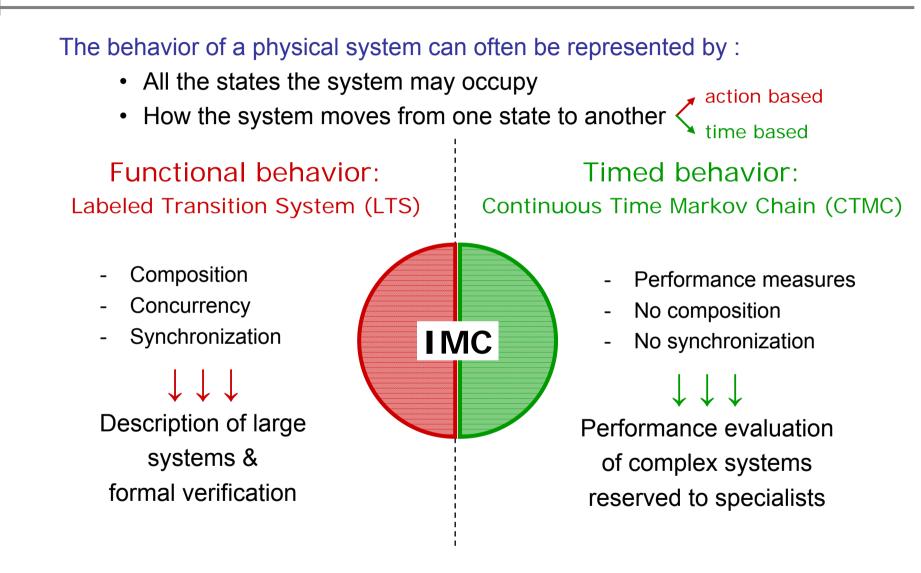


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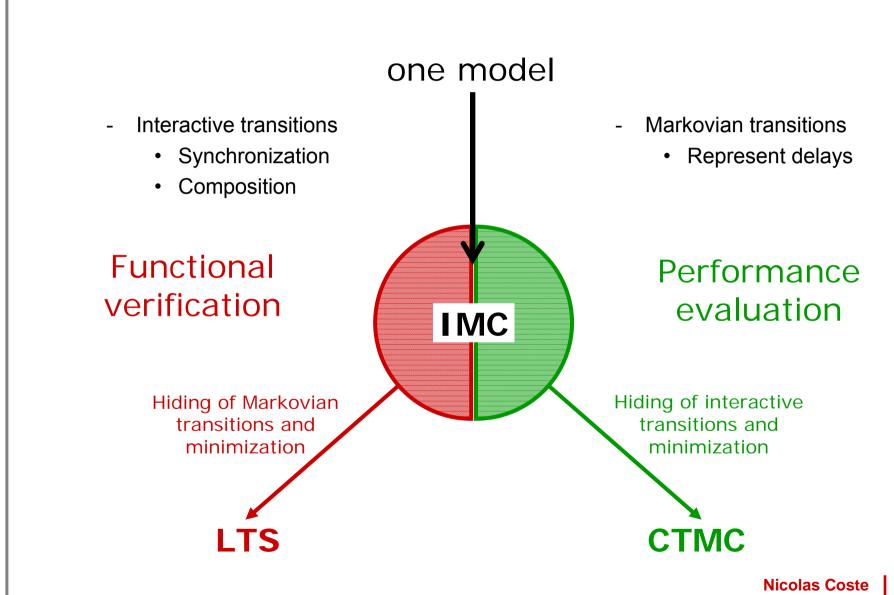
- Interactive Markov Chain (IMC) formalism [Hermanns] -

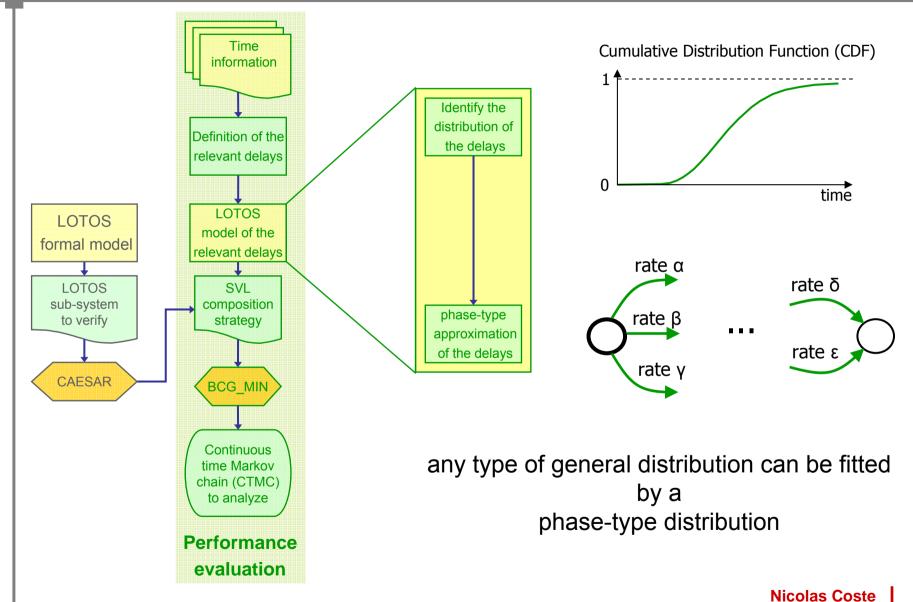


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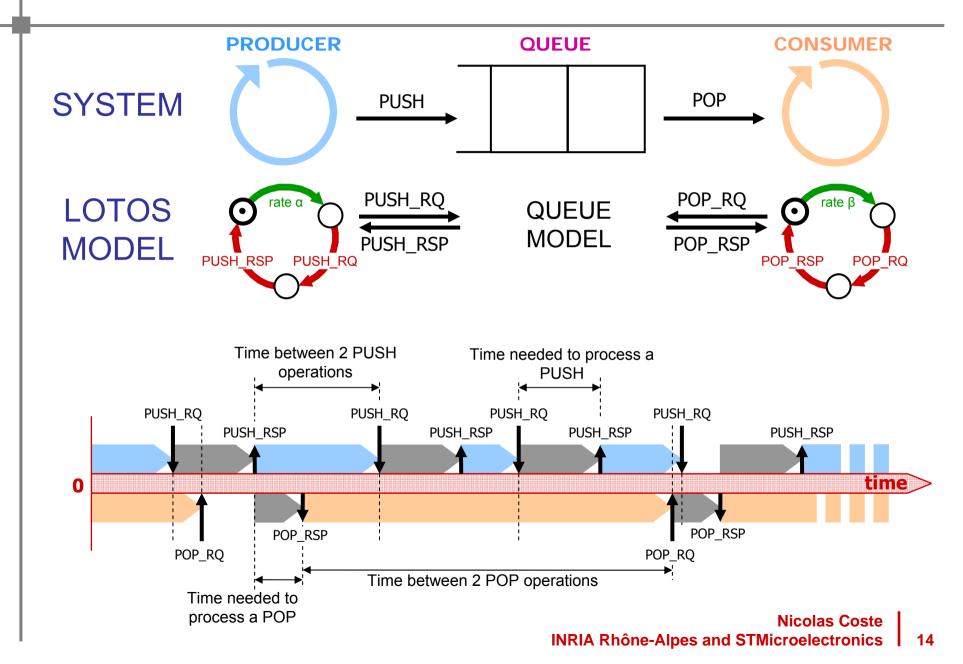


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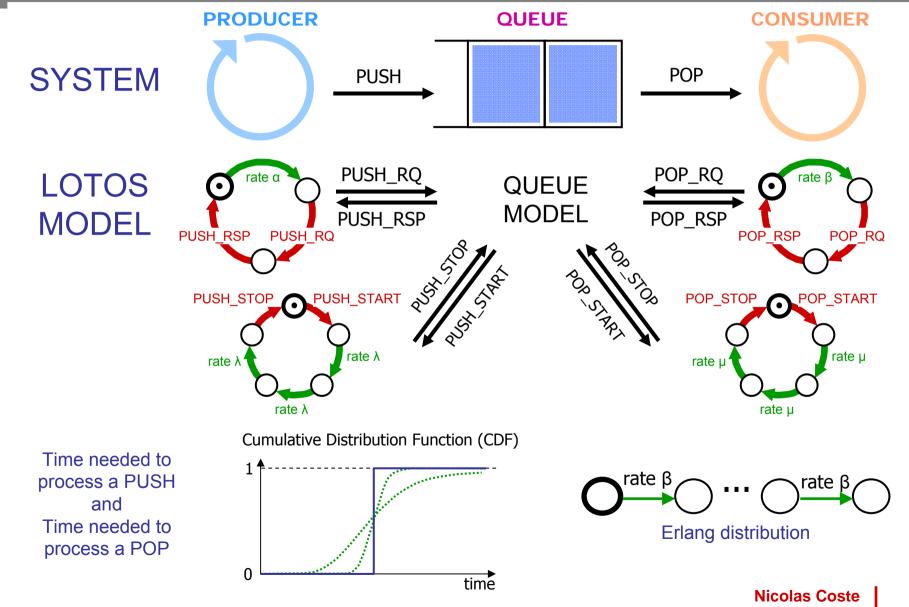




### **Example: a simplified xSTream queue**



### **Example: a simplified xSTream queue**



# Conclusion

Several early results...

- Functional verification
  - Two functional issues highlighted in xSTream
  - Formal verification of the FAUST NoC router
  - Theoretical results on isochronous forks in asynchronous circuits
- Performance evaluation
  - Prediction of latencies of an MPI benchmark on the FAME2 architecture for different topologies, different software implementations of the MPI primitives and different cache coherency protocols.
  - Possibility to predict latencies, throughputs and queue occupancy in the xSTream architecture.

# Conclusion

... but nothing can be taken for granted.

- Functional verification
  - 2 different approaches (top-down and bottom-up)
  - But we are never sheltered from state explosion  $\rightarrow$  expertise is needed !

#### Performance evaluation

Trade-off between good phase-type approximation and state explosion No knowledge of the accuracy gain due to a better phase-type approximation